REMARKS

Applicants respectfully request reconsideration of this application as amended.

Office Action Rejections Summary

Claims 1, 7 and 19 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,198,751 of Dorsey et al. ("Dorsey").

Claim 13 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Dorsey.

Claims 2-6, 8-12 and 14-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Dorsey in view of U.S. Patent No. 6,181,694 of Pickett ("Pickett").

Status of Claims

Claims 1-27 are pending in the application. Claims 1, 5, 7, 11, 13 and 19 have been amended. The amended claims are supported by the specification. Claims 20-27 have been added. No new matter has been added. No claims have been canceled.

Claim Rejections

Claims 1, 7 and 19 have been rejected under 35 U.S.C. §102(e) as being anticipated by Dorsey. Claim 13 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Dorsey.

It is submitted that claim 1 is patentable over the cited reference. Claim 1, as amended, recites:

> A method comprising:
>
> determining whether a **digital signal processor** needs a service program stored in an overlay memory; and
>
> delivering the service program to the digital signal processor from the overlay memory over a **host port interface bus**.

(emphasis added).

The Office Action states:

> Referring to claims 1, 7 and 19, Dorsey discloses determining whether a digital signal processor needs a service program stored in a juke box overlay memory (when a packet arrives at a packet translator, it is determined what set of instructions a controller needs from an opcode memory in order to provide the particular protocol service (see column 4 line 45 through column 5 line 21 and column 7 line 64 through column 8 line 37 and figure 5)) and delivering the service program to the digital signal processor from the juke box overlay memory over a host port interface bus (the appropriate opcode instructions form the opcode memory are sent **to the controller** over **a bus** (see column 4 line 45 through column 5 line 21 and column 7 line 64 through column 8 line 37 and **item 16 in figure 5**)).

(Office Action, 9/29/04, p. 2)(emphasis added)

Applicants respectfully disagree with the Office Action's characterization of Dorsey. At the passages cited to by the Office Action, Dorsey discloses that an opcode memory 51a stores various instructions required for all of the translations that the MPT is capable of performing. Instructions are fed from the opcode memory 51a to the pipeline unit 52. The pipeline unit is implemented using 8 bit register banks as illustrated in FIG. 6. At the beginning of the translation process, the controller 24 of FIG. 2 selects the appropriate microcoded instructions stored in the opcode memory 51a for use in the applicable translation (i.e., depending on the original and the new protocol for the translation). The controller 24 sets the address control 51b to the appropriate start place for the translation process. Dorsey further discloses that the controller 50 can be implemented using discrete components or as part of an ASIC or using programmable logic arrays. The controller 50 may also be implemented using a general purpose central processing unit, although this level of complexity may not be necessary for many implementations. (Dorsey, col. 8, lines 2-37; Figs. 5 and 6).

It is submitted that the controller 50 of Dorsey is not a "digital signal processor" as purported by the Office Action. Although Dorsey discloses that controller 50 may be an ASIC, a PLD, or a general purpose CPU, Dorsey does not disclose that controller 50

may be implement using a DSP. A DSP is a heterogeneous architecture from that of an ASIC, PLD or general purpose CPU, as is well known in the art (See e.g., Different Device Types, techBites INTERactive, 2001 – submitted in an IDS filed herewith).

Furthermore, claim 1 does not recite a "bus" but, rather, a "host interface bus." It is submitted that the bus of Figure 5 of Dorsey is not a host port interface bus, as purported by the Office Action. Nothing in Dorsey discloses or teaches the use of a host port interface bus. If the Examiner continues to purport such a disclosure, the Examiner is respectfully requested to more precisely identify the column and line number in Dorsey where such may be found.

In contrast to Dorsey, claim 1 includes the limitations of delivering a service program to a "digital signal processor" from an overlay memory over a "host port interface bus." Nothing in Dorsey discloses the above noted claim limitations. Therefore, it is submitted that claim 1 is patentable over Dorsey.

For reasons similar to those given above with respect to claim 1, it is submitted that claims 7, 13 and 16 are patentable over Dorsey.

Claims 2-6, 8-12 and 14-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Dorsey in view of Pickett. Claims 2-6, 8-12 and 14-18 depend from and include the limitations of their respective independent claims 1, 7 and 13. It is submitted that Pickett fails to cure the deficiency noted above with respect to Dorsey. Therefore, it is submitted that claims 2-6, 8-12 and 14-18 are patentable over the cited references.

In conclusion, applicants respectfully submit that in view of the arguments set forth herein, the applicable rejections have been overcome.

If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Daniel Ovanezian at (408) 720-8300.

If there are any additional charges, please charge our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 12/20, 2004

Daniel E. Ovanezian
Registration No. 41,236

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300

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